Report on Timing and TWSTFT Activities

at

TimeTech, Stuttgart

Wolfgang Schäfer

e-mail: wolfgang.schaefer@timetech.de

web: www.timetech.de

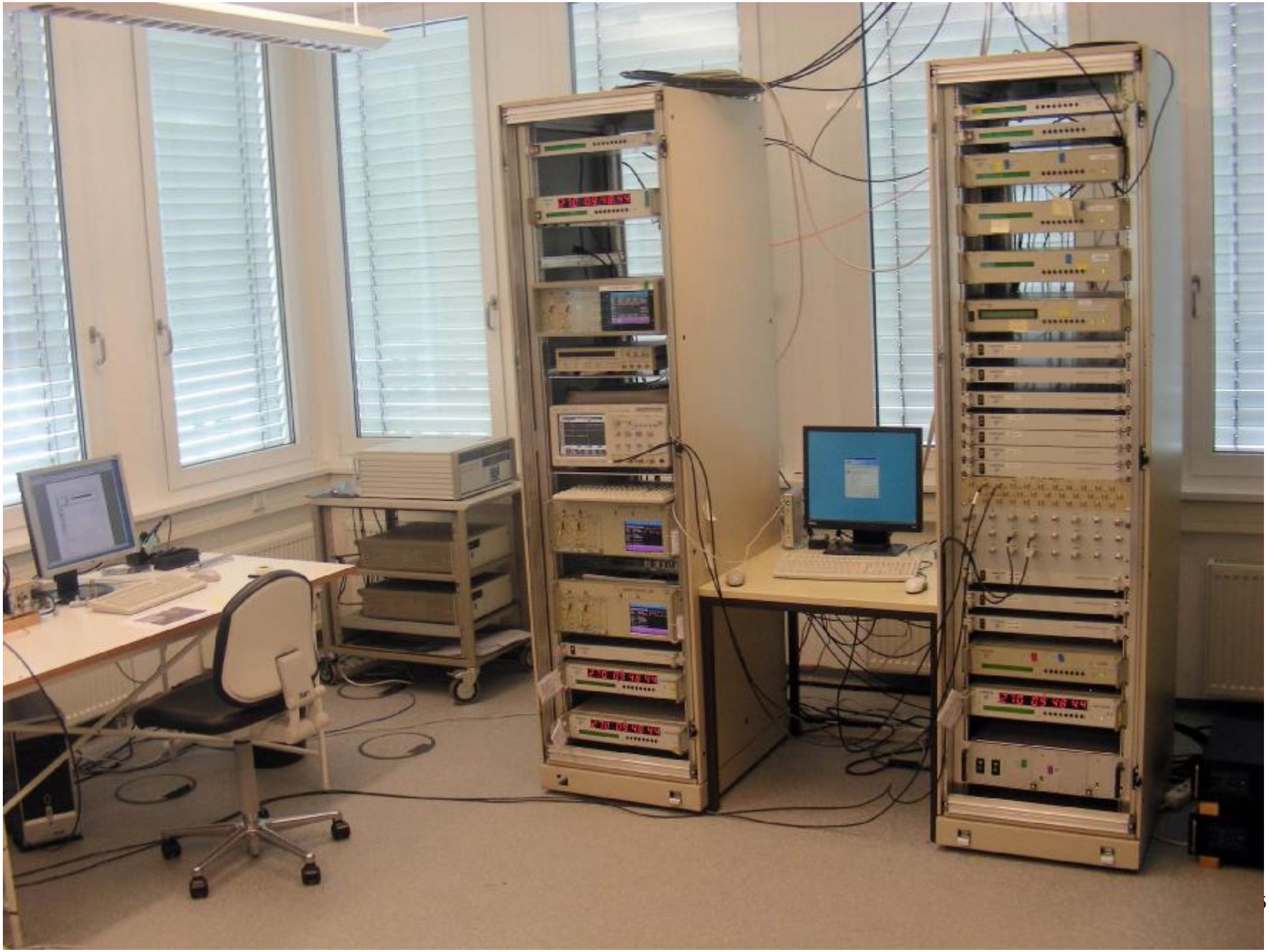
TimeTech GmbH
Curiestrasse 2
D-70563 Stuttgart
Germany

Phone: +49-711-678 08-0
Fax: +49-711-678 08 99

Table of contents

1. TimeTech's link to UTC

- Set up a small Time-Lab to get "hands- on experience" (non-NMI)
- Operate own equipment as well as that from other manufacturers
- Start calibration to UTC, evaluate calibration procedures
- Get experience, how to start and set-up a time-lab from scratch
- Learn, how to tune clocks, how to characterise clocks etc…
- Learn about operational characteristics of time-comparison equipment
- Perform TWSTFT calibration prior to shipment
- Validate GPS receivers and clocks prior delivery to customers
- 2 TTS-3 receivers have been evaluated & calibrated together with PTB



Equipment

- 1 station operational to EU (US not implemented, no WG switch), w. SATSIM
- 1 station set-up to start a link to Asia, w. SATSIM
- 1 PHM VCH-1006, Vremycha
- 2 Cs high performance tubes, Agilent, one clock is nearly as good as the PHM
- 1 Three-channel SATRE, w. SATSIM & Antenna Signal Distribution
- 2 Two-channel modems
- 7 GPS all-in-view: UT oncore TDEV 1.5ns @ 1 day for single receiver, like a Cs!
- Various time interval counters (built into most of our equipment)
- 4 Time-Scale generators, using 1pps, 10 MHz and 100 MHz
- Data-collection server
- Use UDP data broadcast to Data Collection Server & MySQL data base
- Software for off-line data evaluation

Ready for operation and dedicated experiments

2. DLL Characteristics & possible deficiencies

1. Delay vs. Signal Amplitude

- Un-calibrated effect: 30ps/dB calibrated since ~5 years

2. Delay vs. a-symmetric interference

- Effect present, when interferer is off the centre frequency
- Independent of modulation
- Interferer must have significant higher power (10..20 dB above signals)
- SATRE inputs filter has 7 MHz of BW (slightly a-symmetric itself!)
- Error proportional to interferer power and proportional to frequency offset
- Un-calibrated effect: up to 1..2ns calibrated since ~5 years

3. "Characteristic Link Offset"

- Observed first in the "PRARE" Ranging System, using 4 different calibrated receiver channels observing the same ground station
- Analytical approach using simulation of DLL and Link imperfections
- Observed effect occurs only in combination of

  - DLL (phase or amplitude) balance between early and late is imperfect
  - the received signal spectrum is not symmetric in upper and lower side-band

- Result: Characteristic bias for each combination of

  - non-ideal DLL and non-ideal signal transmitter & signal path

- The bias is very constant, no variations detectable, may be calibrated
- Solution: tune phase imbalance in the two DLLs (same as for asym. Interferer)
- MITREX has a RF output filter, resulting in potentially large biases (OCA ?)
- SATRE uses base-band filtering, with nicely symmetric output spectrum

- Effect is detectable using a special version of SATRE “Downconverter” module,

  using side-band inversion (experiments?)
  use SATRE wide-band input filter

- Operate a time link in two sessions with and without sideband inversion
- Evaluate both results
- The AVERAGE of both should be right solution

Remarks:

- Exercise caution when adding Tx output filters to Modems
- Observe spectral symmetry
- Check for good and stable input- output impedance match

4. Coherent interference

- Signals leaking from transmitter to receiver
- All signals on the “same” frequency on the transponder
- Try offsetting transmitted carrier frequencies, by few 10 Hz .. 100 Hz

3. Conclusions / Outlook: Possible 2-way Improvements & Experiments

UDP data output & data collection servers, real-time solution

SATSIM: delay instability at elevated temperature: NEW TRANSCEIVER (Anacom?)

Inverted Sidebands: requires special down-converters, can be re-fitted

Offsetting of transmitters

Real-time TWSTFT: include REFDELAY in the real-time data exchange (in 2008)

TWSTFT networking: remote monitoring & control

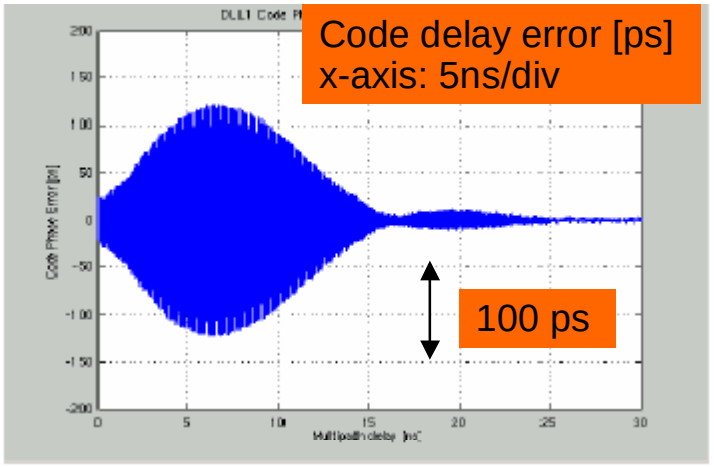
Carrier Phase: Sent a data-package containing all “know-how” to PTB

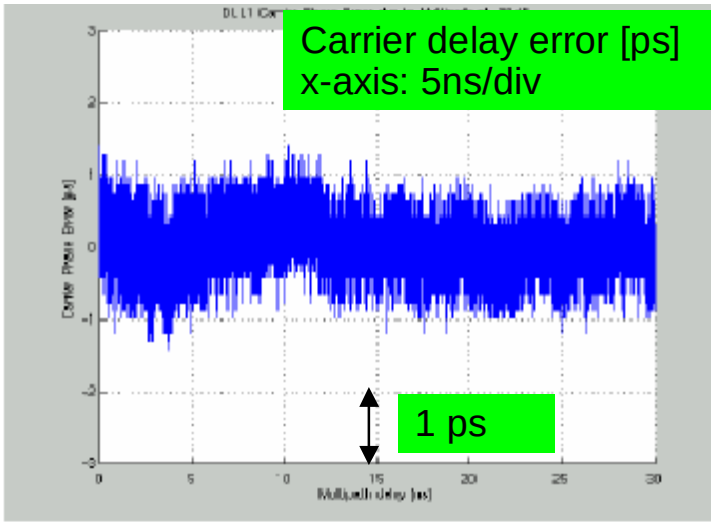
- No detailed work yet due to lack of resources
- Encouraging results from ACES MWL work on H/W and multipath

Carrier phase is definitely more stable compared to the modulation phase

Common-Clock and simultaneous links towards Asia and EU-US

Mutipath Tests @ 100 MChip/s





Test Condition

- MP signal at – 30 dBc
- MP delay shifted from 0 to 3 chips, 0..30ns
- Code / Carrier phase error vs MP delay

Top: Code Delay ERROR

- Dramatic and fast variations (>200ps)
- Code highly affected by carrier phase
- PN suppresses PM for delays > 1.5 Chip-length

Bottom: Effect on Carrier Phase

- Happily, only slight effect visible (< 1 ps)